

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

- 1) (currently amended) A circuit capable to receive an input signal having a duty-cycle, comprising:
 - a first sampler capable to obtain a first edge value from the input signal responsive to an edge clock signal;
 - a second sampler capable to obtain a first data value from the input signal responsive to a data clock signal; and,
 - a duty-cycle-correction logic, coupled to the first and the second samplers, capable to generate a duty-cycle-correction signal that adjusts the edge clock signal to the duty-cycle of the input signal duty-cycle responsive to the first edge value and first data value.
- 2) (original) The circuit of claim 1, wherein the data clock signal has an approximate 50% duty-cycle and is in quadrature with an adjusted edge clock signal.
- 3) (original) The circuit of claim 1, further comprising:
 - a third sampler, coupled to the duty-cycle-correction logic, capable to obtain a second data value; and,
 - wherein the duty-cycle-correction logic is capable to generate the duty-cycle-correction signal responsive to the first data value, first edge value and second data value.
- 4) (currently amended) The circuit of claim 3, wherein the duty-cycle-correction logic comprises:
 - an evaluator circuit capable to generate at least one of an up signal ~~or~~ and a down signal, responsive to the first data value, first edge value and second data value; and,
 - a duty-cycle clock integrator, coupled to the evaluator circuit, capable to generate the duty-cycle-correction signal responsive to the at least one of the up or and down signal.

- 5) (original) The circuit of claim 4, further comprising:
a first phase comparator, coupled to the first sampler, capable to generate the data clock signal; and,
a second phase comparator, coupled to the first duty-cycle clock integrator and the second sampler, capable to generate the edge clock signal responsive to the duty-cycle-correction signal.
- 6) (original) The circuit of claim 1, wherein the input signal is a double-data rate signal and the circuit is included in a double-data rate system.
- 7) (original) The circuit of claim 1, wherein the circuit is included in a memory module coupled to a double-data rate bus.
- 8) (currently amended) A circuit capable to receive an input signal having a duty-cycle, comprising:
a first sampler capable to obtain a first edge value from the input signal responsive to an edge clock signal;
a second sampler capable to obtain a second edge value from the input signal responsive to the edge clock signal; and
a duty-cycle-correction logic, coupled to the first and the second samplers, capable to generate a duty-cycle-correction signal that adjusts the edge clock signal to the duty-cycle of the input signal duty-cycle responsive to the first and second edge values.
- 9) (original) The circuit of claim 8, wherein a data clock signal has an approximate 50% duty-cycle and is in quadrature with an adjusted edge clock signal.
- 10) (currently amended) The circuit of claim 8, wherein the duty-cycle-correction logic comprises:
an evaluator circuit capable to generate at least one of an up signal or a down signal, responsive to the first and second edge values; and,

a duty-cycle clock integrator, coupled to the evaluator circuit, capable to generate the duty-cycle-correction signal responsive to the at least one of the up and ~~or~~ down signal.

- 11) (original) The circuit of claim 10, further comprising:

a first phase comparator, coupled to the duty-cycle clock integrator and the first and second samplers, capable to generate the edge clock signal responsive to the duty-cycle-correction signal.

- 12) (original) The circuit of claim 8, wherein the input signal is a double-data rate signal and the circuit is included in a double-data rate system.

- 13) (original) The circuit of claim 8, wherein the circuit is included in a memory module coupled to a double-data rate bus.

- 14) (original) A circuit capable to receive an input signal having a duty-cycle, comprising:

a first sampler capable to obtain a first edge value from the input signal responsive to an edge clock signal;

a second sampler capable to obtain a second edge value from the input signal responsive to the edge clock signal;

a duty-cycle-correction logic, coupled to the first and the second samplers, capable to generate a duty-cycle-correction signal that adjusts the edge clock to the duty-cycle of the input signal responsive to the first and second edge values;

wherein the duty-cycle-correction logic includes,

an evaluator circuit, coupled to the first and second samplers, capable to generate an adjust signal, responsive to the first and second edge values;

a counter, coupled to the evaluator circuit, capable to output a count value responsive to the adjust signal;

a digital-to-analog-converter, coupled to the counter, capable to generate an analog offset signal responsive to the count signal; and,

a duty-cycle clock integrator, coupled to the digital-to-analog-converter, capable to generate the duty-cycle-correction signal responsive to the analog offset signal.

- 15) (original) The circuit of claim 14, wherein a data clock signal has an approximate 50% duty-cycle and is in quadrature with an adjusted edge clock signal.
- 16) (original) The circuit of claim 14, further comprising;
a digital filter coupled to first and second samplers and the evaluator circuit.
- 17) (original) The circuit of claim 16, wherein the input signal is a coded input signal having an approximate same number of even and odd data transitions.
- 18) (original) The circuit of claim 14, further comprising:
a first phase comparator, coupled to the duty-cycle clock integrator and the first and second samplers, capable to generate the edge clock signal responsive to the duty-cycle-correction signal.
- 19) (original) The circuit of claim 14, wherein the input signal is a double-data rate signal and the circuit is included in a double-data rate system.
- 20) (original) The circuit of claim 14, wherein the circuit is included in a memory module coupled to a double-data rate bus.
- 21) (original) An apparatus, comprising:
a transmit circuit capable to transmit a serial signal having a duty-cycle;
a receive circuit, coupled to the transmit circuit, including
a first sampler capable to obtain a first edge value from the serial signal responsive to an edge clock signal;
a second sampler capable to obtain a first data value from the serial signal responsive to a data clock signal; and,

a duty-cycle-correction logic, coupled to the first and the second samplers, capable to generate a duty-cycle-correction signal that adjusts the edge clock signal to the duty-cycle of the serial signal duty-cycle responsive to the first edge value and first data value.

22) (original) An apparatus, comprising:

a transmit circuit capable to transmit a serial signal having a duty-cycle; and,
a receive circuit, coupled to the transmit circuit, including

a first sampler capable to obtain a first edge value from the serial signal responsive to an edge clock signal;

a second sampler capable to obtain a second edge value from the serial signal responsive to the edge clock signal; and,

a duty-cycle-correction logic, coupled to the first and the second samplers, capable to generate a duty-cycle-correction signal that adjusts the edge clock to the duty-cycle of the serial signal duty-cycle responsive to the first and second edge values.

23) (original) An apparatus, comprising:

a transmit circuit capable to transmit a serial signal having a duty-cycle; and,
a receive circuit, coupled to the transmit circuit, including,

a first sampler capable to obtain a first edge value from the serial signal responsive to an edge clock signal;

a second sampler capable to obtain a second edge value from the serial signal responsive to the edge clock signal;

a duty-cycle-correction logic, coupled to the first and the second samplers, capable to generate a duty-cycle-correction signal that adjusts the edge clock to the duty-cycle of the serial signal responsive to the first and second edge values;

wherein the duty-cycle-correction logic includes,

an evaluator circuit, coupled to the first and second samplers, capable to generate an adjust signal, responsive to the first and second edge values;

a counter, coupled to the evaluator circuit, capable to output a count value responsive to the adjust signal; and,

a digital-to-analog-converter, coupled to the counter, capable to generate the duty-cycle-correction signal responsive to the count signal.

- 24) (currently amended) A method, comprising the steps of:
- receiving an input signal having a first duty-cycle;
 - sampling the input signal to obtain a plurality of edge values from the input signal responsive to an edge clock signal having a second duty-cycle; and,
 - adjusting the second duty-cycle of the edge clock signals to the first duty-cycle of the input signal responsive to the plurality of edge values.
- 25) (original) The method of claim 24, further comprising the steps of:
- sampling the input signal to obtain a plurality of data values from the input signal responsive to a data clock signal.
- 26) (original) The method of claim 25, wherein the adjusting step includes adjusting the data clock signal to have an approximate 50% duty-cycle and be in quadrature with an adjusted edge clock signal.
- 27) (original) A circuit capable to receive an input signal having a duty-cycle, comprising:
- a sampler capable to obtain a plurality of edge values from the input signal responsive to an edge clock signal having a duty-cycle; and,
 - means, coupled to the sampler, for adjusting the edge clock signal duty-cycle to the input signal duty-cycle.